Configurable Heat Generators for FPGAs

Paweł Weber[1], Maciej Zagrabski[1], Przemysław Musz[1], Krzysztof Kępa[2], Maciej Nikodem[1], Bartosz Wojciechowski*[1]

[1]Institute of Computer Engineering, Control and Robotics, Wrocław University of Technology, Wrocław, Poland

[2]Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA

* Corresponding Author: bartosz.wojciechowski@pwr.edu.pl, tel.: +48 71 320 2873, fax.: +48 71 320 2677

Abstract

This work describes methodology for implementation of high-performance synthetic heat generators within the FPGA fabric. The proposed design flow is compatible with vendor tools and the generated synthetic heat generators can be seamlessly integrated with existing designs. Various architectures of synchronous and asynchronous heaters are evaluated in terms of their efficacy and dynamic range. We provide temperature and power measurements of the heaters implemented in Virtex5 FPGA. Measuring power consumption allows to validate heater performance and the extent to which its power dissipation can be controlled.

1 Introduction and Related Work

Due to advances in technology modern FPGAs fabricated in nm-scale technologies provide large amounts of configurable logic and many specialised blocks suitable for implementation of System-on-Chip designs. This, however comes at the cost of high power densities and elevated temperature levels. Temperature adversely impacts leakage power, device speed, package design costs and device lifetime. Therefore researcher attention is directed at measurements and simulation of temperature of such devices. Also, by measuring response of the device to artificial thermal stimuli details about chip- to-ambient structure of the package can be extracted. This way thermal behaviour of the whole device can be characterised and predicted [1] as well as thermal simulators validated [2]. Another application of heating elements is for thermal-aware testing [3] where self-heating allows circumventing the limitations of the temperature-controlled chamber. In this work we are proposing design of various configurable heat generators to be able to precisely heat up an FPGA. Also we describe EDA tools for automated DUT instrumentation with such artificial heaters and run-time control of their operation.

To date the best performing heaters in terms of raw power density could be obtained in FPGAs by configuring their Look-Up Tables (LUTs) to operate as a set of 1-stage Ring Oscillators [4, 5]. However, RO architecture is sensitive to voltage level changes, which is not the case for synchronous heaters. Hence, we compare RO-based approach and performance with a range of synchronous designs. Our heater designs target Spartan 3E, Spartan 6 and Virtex-5 devices, but our toolset can be easily expanded for support of other Xilinx FPGA families.

In previous research on synthetic heat sources, e.g. [6, 7] the fast-switching FPGA user logic resources (RO's and shift registers) were used as a main heat source. Such approach is straightforward and can be implemented using vendor tools. However using automated placer and router reduces the level of control on placement of the heaters. Also some heater configurations are not allowed by the synthesis tools and can be removed during optimization. For this reason we operate on the XDL-level of description of internal configuration of the device [8]. The vendors router is used only to connect our heaters to the control logic.

Some researchers brought up several doubts regarding the accuracy of temperature sensors within the FPGA [9]. Thus, in order to correctly evaluate the performance and quality of proposed heaters we rely mostly on power consumption measurements. Also with large heaters the whole board heats up and it is non-trivial to put the FPGA in a thermal steady-state. Hence, the temperature measurements may not be repeatable. For these reasons we limited the heater size so that obtained results remain within the temperature limits where temperature sensors operate well.

Contribution

The main contributions of this work are the following: i) a robust methodology for comparing FPGA-compatible heaters in terms of not only maximal temperature, but also power dissipation and power density, ii) update to our toolset with automatic configuration of heaters for Vitex 5 FPGA-based platform. To the best of our knowledge, power measurements of heaters in FPGAs have not been published before.

2. Methodology

Heater configuration and automatic placement

For automatic placement of heaters we use the toolset previously presented in [5]. The main improvement is that now toolset supports widely used Virtex-5 device family that facilitates direct and fair comparison with other research groups. Additionally the number of available heater types

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has increased as well as frequency generators were added to allow for the use of synchronous heaters.

Since each basic heater element can be placed in a single CLB our approach to heater configuration and placement provides both flexibility and control. Also it yields high power density as the toolset makes sure that all CLBs in a selected area are configured as heaters.

Heater types

We implemented both asynchronous (Fig. 1) and synchronous heaters (Fig. 2). The asynchronous heaters use one and three-stage oscillators since longer inverter chains lower oscillation frequency and hence, power density drops significantly.

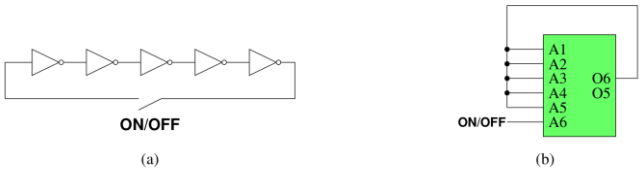

Figure 1. Idea and implementation of heater based on Ring Oscillators (RO).

Four basic synchronous heater types use Inverter Buffers (IB), Flip-Flops (FF), Shift Registers (SR) and Flip-Flop Pipelines (FFPL). Since synchronous heaters need clock source – we implemented frequency generators providing 100, 200, 300 and 350 MHz switching/clock signal. Use of faster frequency sources is counterproductive with most heaters since they don't switch fast enough. This was previously demonstrated [7] and was confirmed by our experiments (see Tab. 1).

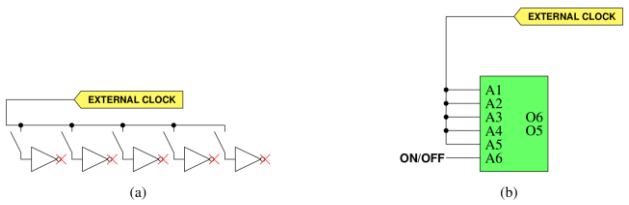

Figure 2. Schematic and implementation of Inverter Buffer heater

Proposed heaters are organized and controlled in groups called Logical Heaters (LH). Each consists of at least one Basic Heater (BH). Single BH occupies only one CLB. Such design provides flexibility and ultimate fine-grained control of heater size and placement. To limit complexity our tools allow only for one type of BH (RO1, RO3, FF, SR, IB or FFPL) within each LH, but every LH group can contain different type of BH. Heater layout is defined in XML configuration file and the exact routing within each BH type is stored in a database. The database holds complete *netlist* of each single basic heater type. Therefore, heaters with uniform parameters are placed automatically on the FPGA die and routed as defined in configuration files. The radiated power output of each LH can be controlled by Pulse Width Modulation (PWM). Also, for all synchronous heaters the amount of dissipated power can also be controlled through frequency of clock signal. Each synchronous heater can use different frequency source.

Temperature measurement

We use Xilinx SystemMonitor connected to the SimulationCore IP as the main temperature measurement method. We augment it with a grid of RO-based sensors as described in [5]. We have also used external Pt100 temperature probe connected to Agilent 33410A multimeter. The temperature sensor is placed in the middle of the heatsink for a reference temperature measurement.

Power measurement

Power consumption of all heater types was measured indirectly by measuring total current flow at Vcc pin from the DC/DC converter powering the FPGA core. To do that we measure the voltage drop V_{track} on a PCB track between the power converter's onboard inductor and the output pin of the DC/DC. To calculate the resistance of the track we apply an auxiliary current sink that can be turned on and off and its current I_{load} can be precisely measured. With additional current sink we measure an increased voltage drop V_{load}. Having this data we calculate total power consumption of the FPGA according to (1).

$$P_{FPGA} = \frac{V_{track} \cdot V_{cc} \cdot I_{load}}{V_{load} - V_{track}} \qquad (1)$$

With all heaters except from type *RO1* (1-stage ring oscillator) the supply current value was low enough not to change track temperature enough to affect the resistance of the PCB track significantly. Also with low overall power consumption, the core voltage drop that we noticed was not higher than 0.02 V. Therefore, the power measurement results of all heaters except the RO1 can be considered accurate. The measured track resistance in room temperature was 0.15 Ohm, with standard deviation of 0.0024. The extreme case of increase of path resistance with temperature due to self-heating is shown in Figure 3.

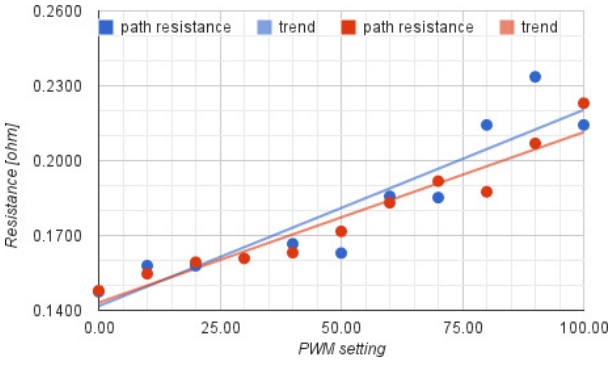

Figure 3 Path resistance changes with RO1 heater PWM due to current-induced heating.

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3. Experimental Evaluation – Results

All tests were performed using Xilinx XUPV5 board (Virtex-5 LX110T FPGA) [10]. To exclude inter- and intra-device variation we measured various heater configurations on four different devices. The relative performance of the heaters was evaluated by measuring power consumption as well as temperature increase within the FPGA fabric. For that purpose a grid of temperature sensors [5] has been placed among the heaters.

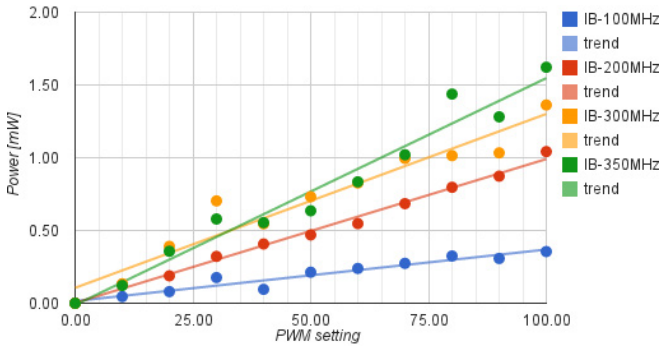

Figure 4. Measured power of one basic heater based on Inverter Buffer as a function of clock generator and PWM setting.

Since the steady-state temperature and the dynamic temperature response to a synthetic heat source depend on the ambient conditions, unlike the authors of [4], we value more the power consumption results. Apart from maximal heater power output and temperature increase we measured power as a function of heater size and PWM settings. This was done in order to rule out any negative effects such as load-induced IR drop or limited power output of the DC-DC converter that would otherwise impact the results.

The power measurement and temperature increase results are presented in Tab 1. For each heater type we created a single heater consisting of 1480 BHs (17.1 % of all CLBs on the chip) and measured the maximal power consumption per CLB and maximal increase over the base (ambient) temperature. It is important to note that RO1 heaters are the most potent, easily causing overheating and core voltage swings that can cause the device reset. From the synchronous heaters those based on inverter buffers and flip-flops are the best performing. However, it has to be noted that due to limits in switching speed the FF heaters do not operate correctly above 300 MHz, and FFPL heaters' power output drops with frequencies over 200 MHz.

Table 1: Heater comparison table. Each heater occupies 1480 CLBs in 25 columns and 60 rows. For synchronous heaters values for 100, 200, 300 and 350 MHz clock generators are given.

Heater pe	Power per CLB [mW]	Temp increase [K]	Comment
RO1	**7.5**	**> 150 C**	**device reset due to overheating**
RO3	**0.81**	**8**	**-**
IB	**0.36; 1.04; 1.36; 1.62**	**7.6, 12.3, 17.6; 19.0**	**require external clock generator**
SR	**0.07; 0.12; 0.19; 0.21**	**1; 1.5; 2.5; 4**	
FF	**0.65; 1.07; 1.51; 0.56**	**6.5; 12; 17; 6.0**	
FFPL	**0.46; 0.81; 0.68; 0.62**	**5.5; 7; 12; 12.5**	

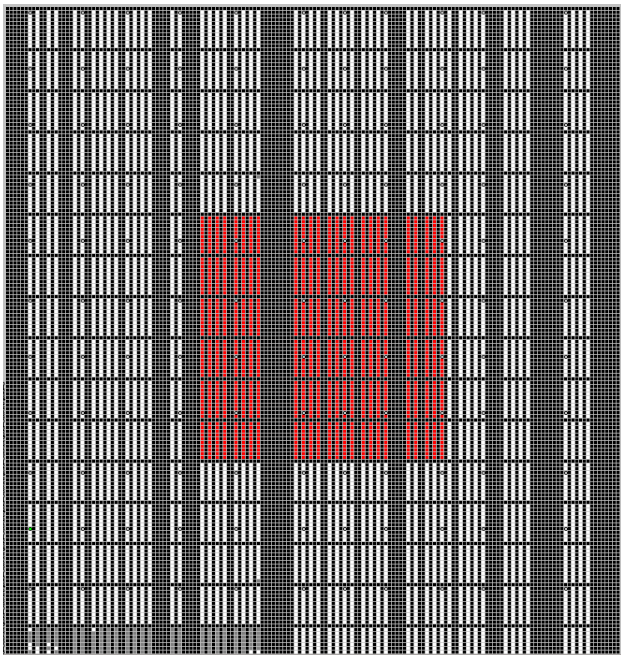

Figure 5. Placement of measured heater (red area in the center) and control logic – SimulationCore (gray rectangle in lower left corner).

Fig 6 illustrates the observed increase in the temperature measured by the embedded SystemMonitor and by the external resistance thermometer. It can be observed that temperature swing with respect to idle temperature increases with higher frequency of the generator. The downside of using higher frequency generators is thus the increase of idle temperature caused by dynamic power consumption in the

clock distribution network and the parts of the heaters that are not blocked by the enable signal.

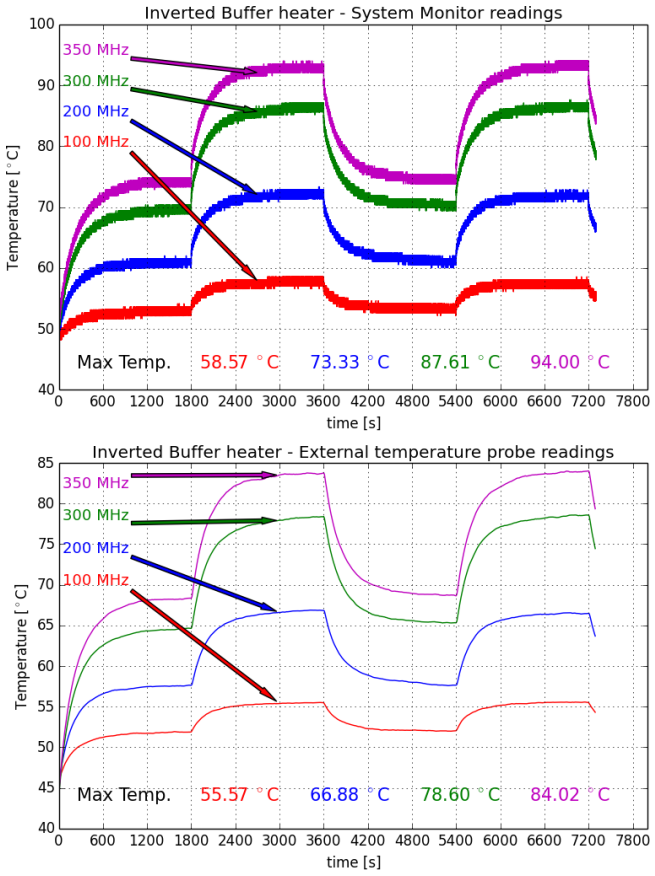

Figure 6. Temperature profiles of the FPGA with IB heater using various clock generators measured with the SystemMonitor and external sensor.

4. Conclusion and future work

In this work we described an updated methodology of configuring and placing artificial heat generating blocks in FPGA matrix that are suitable for a wide range of thermal related research. We keep netlists of Basic Heaters occupying only one CLB in a database, and based on configuration in XML file we place them on the FPGA by means of manipulating the low level description of reconfigurable resources. We provided measurement results of power dissipation and temperature increase over ambient conditions for various heater types.

The best performing asynchronous heaters are based on short, one-stage ring oscillators (Fig. 1). Synchronous heaters characterized by the highest power density utilize inverter buffers (Fig. 2). Presented toolset operates directly on FPGA routing and logic primitives, below the HDL-level. Apart from the resources occupied by the heaters and a fixed amount needed by control logic no other resources are used.

Moreover the fine-grained, CLB-accurate heater placement is entirely under User control as the tools place each basic heater into CLB separately.

In future work we will investigate a new architecture of the artificial heat generators using the dynamic leakage in the massive FPGA routing resources as the heat source.

Acknowledgements

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